



arrangement with respect to the interdigitated electrode (4) below the dielectric (3).

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REMARKS

Claim 2 has been cancelled without prejudice.

Claim 1 has been amended to define the invention more clearly in accordance with the figures of the drawing and the descriptions of these figures on page 3, line 5- page 6, line 19 of the specification.

The rejection of Claims 1 and 5 under 35 U.S.C. 102(b) as anticipated by Ritchie et al. is considered to lack merit.

Unlike the capacitor defined by the instant claims, in the capacitor of the Ritchie et al. patent the interdigitated electrode (14a) that is positioned above the dielectric (13) overlaps the interdigitated electrode (12a) that is positioned below the dielectric.

The rejection of Claim 3 under 35 U.S.C. 103(a) as unpatentable over Ritchie et al. is considered to lack merit. For reasons given in regard to parent Claim 1 the Ritchie et al. patent is not considered to even suggest the capacitor defined by Claim 3.

The rejection of Claim 4 under 35 U.S.C. 103(a) as unpatentable over Ritchie et al. in view of Matsubara et al. is considered to lack merit.

For reasons given in regard to parent claim 1 the Ritchie et al. patent is not considered to even suggest the capacitor defined by Claim 4.

The Matsubara et al. patent is not considered to fill in the above-described gap in the teaching of the Ritchie et al. patent. The Matsubara et al. patent does not even suggest a capacitor having interdigitated electrodes.

An early allowance of the claims and case is requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

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On April 16, 2001

By Norman N. Spain



APPENDIX

1. (Amended) A thin film capacitor comprising a carrier substrate (1), at least two interdigitated electrodes (4, 5), and at least one dielectric (3), characterized in that at least one interdigitated electrode (4) is arranged below the dielectric (3) [and], at least one interdigitated electrode (5) is arranged above the dielectric (3) and the interdigitated electrode (5) above the dielectric (3) is positioned in a staggered, non-overlapping, arrangement with respect to the interdigitated electrode (4) below the dielectric (3).

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